Claims

1. A granular FIFO (fill-in fill-out) fill level indicator system, said system comprising:

a write counter coupled to a write clock, said write counter having a state corresponding to said write clock;

a read counter coupled to a read clock, said read counter having a state corresponding to said read clock;

a plurality of FIFO registers configured to receive a write data and output a read data using said write and read clocks; and

a comparison module configured to determine a fill level of said FIFO registers, said fill level corresponding to a comparison of said write counter state and said read counter state.

2. The FIFO fill level indicator system of claim 1, wherein said write and read clocks are asynchronous.

3. The FIFO fill level indicator system of claim 1, wherein said comparison comprises a difference between said write counter state and said read counter state.

4. The FIFO fill level indicator system of claim 1, wherein said comparison comprises a phase difference between said write counter state and said read counter state and said fill level comprises a number of read counter cycles.

5. The FIFO fill level indicator system of claim 1, wherein said FIFO registers comprise a plurality of digital words and said words correspond to a frequency offset.

6. The FIFO fill level indicator system of claim 5, wherein said frequency offset is used to generate a phase shift in a data clock.

7. The FIFO fill level indicator system of claim 1, wherein said system is configured to maintain said FIFO registers at a constant fill level.

8. The FIFO fill level indicator system of claim 1, wherein said comparison module comprises a reset counter and a register.

9. The FIFO fill level indicator system of claim 8, wherein said write counter state is used to reset said reset counter.

10. The FIFO fill level indicator system of claim 8, wherein said reset counter is clocked by said read clock and said register is clocked by said read counter state.

11. The FIFO fill level indicator system of claim 1, wherein said comparison module comprises a plurality of phase detectors and a binary decoder.

12. The FIFO fill level indicator system of claim 11, wherein said comparison comprises sampling a phase from one of said phase detectors with a phase from said read counter.

13. A method of indicating a FIFO fill level, said method comprising:

receiving a state of a write counter in a comparison module, said write state corresponding to a write clock;

receiving a state of a read counter in said comparison module, said read state corresponding to a read clock;

receiving a write data in a plurality of FIFO registers and outputting a read data using said write and read clocks; and

determining, in said comparison module, a phase difference between said write state and said read state, wherein said phase difference corresponds to said FIFO fill level in said FIFO registers.

14. The method of claim 13, wherein said state receiving steps comprise receiving asynchronously said states.

15. The method of claim 13, further comprising the step of generating a phase shift in a data clock in response to said determining step.

16. The method of claim 13, further comprising the step of maintaining said FIFO registers at a constant fill level.

17. The method of claim 13, wherein said determining step comprises:

asynchronously resetting a reset counter;

clocking said reset counter with said read clock;

clocking a register with said read counter state; and

sampling an output of said reset counter with said read counter state.

18. The method of claim 13, wherein said determining step comprises:

receiving in said comparison module multiple phases of said write counter; and

sampling each of said multiple phases with said read counter state;

19. The method of claim 18, wherein said multiple phases comprises three.

20. A PLL/DLL dual loop data serializer comprising:

a phase lock loop (PLL) including,

a phase frequency detector (PFD) receiving a local clock,

a voltage controlled oscillator (VCO),

a loop filter coupled to said PFD and to said VCO, said loop filter configured to suppress VCO phase noise, and

a phase shifter coupled to said VCO and configured in a feedback loop with said PFD;

a FIFO register receiving a parallel write data input;

a delayed lock loop (DLL) having a digital loop filter coupled to said phase shifter of said PLL;

a FIFO fill level indicator in said DLL and receiving an input signal from said FIFO register, said indicator including,

a write counter coupled to a write clock, said write counter having a state corresponding to said write clock,

a read counter coupled to a read clock, said read counter having a state corresponding to said read clock, and

a comparison module configured to determine a fill level of said FIFO register, said fill level corresponding to a comparison of said write counter state and said read counter state; and

a PISO serializer receiving an input from said FIFO and outputting a serialized data.

21. The dual loop serializer of claim 20, wherein said FIFO register configured to output a read data using said write and read clocks.

22. The dual loop serializer of claim 20, wherein said write and read clocks are asynchronous.

23. The dual loop serializer of claim 20, wherein said comparison comprises a difference between said write counter state and said read counter state.

24. The dual loop serializer of claim 20, wherein said system is configured to maintain said FIFO register at a constant fill level.

25. The dual loop serializer of claim 20, wherein said comparison module comprises a reset counter and a register.

26. The dual loop serializer of claim 20, wherein said comparison module comprises a plurality of phase detectors and a binary decoder.

27. The dual loop serializer of claim 26, wherein said comparison comprises sampling a phase from one of said phase detectors with a phase from said read counter.

28. The dual loop serializer of claim 20, wherein said PLL loop filter comprises a wide bandwidth and said DLL loop filter comprises a narrow bandwidth.

29. A dual loop retimer comprising the data serializer of claim 20.